(A) AMENDMENT OF THE CLAIMS:

1. (Currently Amended) An integrated circuit, comprising logic circuits connected to a plurality of shift register latch scan chains and self-test circuits for testing said logic circuits, said self-test circuits in said integrated circuit comprising:

a pseudo-random pattern generator for generating at least one flat pseudo-random patterns to provide to each of the scan chains;

A plurality of weighting circuits for receipt of the pseudo-random patterns from the pattern geneator, a different one of the weighting circuits associated with each of the scan chains, each weighting circuit having a selectable weight set to provide flat or weighted pseudo-random patterns to the scan chains independently of one another;

a different storage element associated with each of the weighting circuits for receipt and storage of flat and weighted pesudo-random patterns each from its different associated weighting circuit; and

a selection circuit for individually addressing each of the storage elements for selective entry of either a flat or weighted pseudo-random pattern into different shift register latches of said scan chains independently of one another for scanning said weighted pattern to said logic circuits to enable provision of pseuco-random patterns of different weights to different shift register latches in the same scan chain.

2. (Original) An integrated circuit as recited in claim 1, wherein said weighting circuit comprises a weight generating circuit and a weight selecting circuit.

3. (Original) The integrated circuit as recited in claim 1, wherein said weighting circuit includes means for receiving a weighting instruction from an external source to said integrated circuit.

4. (Original) The integrated circuit as recited in claim 1, wherein said storage elements are each a first stage of an associated scan chain.

5. (Currently Amended) The integrated circuit as recited in claim 4, wherein said pseudo- random pattern generator and said weighting patterns, receipts pattern and weighting instructions are from a tester internal to said integrated circuit.

6. The integrated circuit as recited in claim 4, wherein said weighting instruction is generated by a tester external to said integrated circuit.

7. (Original) The integrated circuit as recited in claim 4, further comprising a memory or register array wherein at least a portion of said weighting instruction is stored in said memory array.

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) The integrated circuit of claim 1, wherein said pseudo_random pattern generator is a linear feedback shift register coupled to each of the weighting circuits to provide a flat pseudo_random pattern to each of the weighting circuits.

11. (Previously submitted) The integrated circuit of claim 10, wherein the scan paths contain multiple shift register latch stages SRL_1 to SRL_n each with first and second stages which SRL stages are controlled by an A clock, a B clock and a C_1 clock.

12. (Previously submitted) The integrated circuit of claim 11, wherein the first shift register stage SRL of each scan chain functions as said storage element associated with the scan chain and received at its L_1 latch an input from the associated weighting circuit, an address input from an address decoder of the selection circuit and a w-clock for separately addresssing each of the scan paths to enable entry of data from an associated weighting circuit into the first stage of the scan path on a SRL by SRL of the scan path basis.

13. (Previously submitted) The integrated circuit of claim 12 including means performing the following loading sequence steps individually for each of the plurality of scan paths:

generating the next flat or weighted pseudo-random pattern;

aplying the L1 scan clock (A-clk_ to load all the L! Latches of the register array with flat or weight pseudo-random data from the LFSR;

updating an L1 in any specific SRL1 stage scan path by addresssing the particular L1 latch stage and applying thw w-clock;

loading the L2 latch from the L1 latch (B-clk); and

repeating all the steps until the longest scan chain is loaded.